[11403/84]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Aaron PARTRIDGE et al. For: CRACK AND RESIDUE FREE CONFORMAL DEPOSITED SILICON OXIDE WITH PREDICTABLE AND UNIFORM ETCHING CHARACTERISTICS Filed: November 14, 2003 Serial No.: 10/713,172	Examiner: Francis P. SMITH Art Unit: 1792

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Signature: /Elizabeth Tretter/
Elizabeth Tretter

APPEAL BRIEF PURSUANT TO 37 C.F.R. § 41.37

SIR:

On April 6, 2009, Appellants submitted a Notice of Appeal from the last decision of the Examiner contained in the Final Office Action dated November 7, 2008 in the above-identified patent application.

In accordance with 37 C.F.R. § 41.37, this brief is submitted in support of the appeal of the final rejections of claims 4, 11, 16 to 30, 44, 51 and 56. For at least the reasons set forth below, the final rejections of claims 4, 11, 16 to 30, 44, 51 and 56 should be reversed.

1. REAL PARTY IN INTEREST

The real party in interest in the present appeal is Robert Bosch GmbH ("Bosch"), Postfach 30 02 20, 70442 Stuttgart, Federal Republic of Germany. Bosch is the assignee of the entire right, title, and interest in the present application.

2. RELATED APPEALS AND INTERFERENCES

There are no other prior or pending appeals, interferences or judicial proceedings known by the undersigned, or believed by the undersigned to be known to Appellants or the assignee, Bosch, "which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal."

3. STATUS OF CLAIMS

Claims 1 to 3, 5 to 10, 12 to 15, 41 to 43, 45 to 50, and 52 to 55 are canceled.

Claims 31 to 40 have been withdrawn from consideration.

Claims 4, 11, 44, and 51 stand rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,869,384 (the "Yu" reference) in view of U.S. Patent No. 6,436,790 (the "Ito" reference).

Claims 16 to 18, 22 to 24, 26, 29, and 30 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the "Yu" reference in view of U.S. Patent No. 6,544,898 (the "Polson" reference).

Claims 19 and 25 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of the "Yu" reference, the "Polson" reference, and United States Patent No. 5,256,247 (the "Watanabe" reference).

Claims 20 and 21 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of the "Yu" reference, the "Polson" reference, the "Watanabe" reference, and United States Patent No. 5,990,019 (the "Torek" reference).

Claims 27, 28, and 56 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of the "Yu" reference, the "Polson" reference, the "Watanabe" reference, the "Torek" reference, and United States Patent No. 5,904,570 (the "Chen" reference).

Appellants appeal from the final rejections of claims 4, 11, 16 to 30, 44, 51, and 56.

A copy of the appealed claims 4, 11, 16 to 30, 44, 51, and 56 is attached hereto in the Claims Appendix.

4. STATUS OF AMENDMENTS

In response to the Final Office Action dated November 8, 2008, Appellants filed an Amendment After A Final Office Action on February 17, 2009 and a Supplemental Amendment After Final Office Action ("Supplemental Amendment") on April 6, 2009. The Supplemental Amendment canceled claims 1 to 3, 5 to 10, 12 to 15, 41 to 43, 45 to 50, and 52 to 55, and amended claims 4, 44, and 51 The second Advisory Action, dated April 22, 2009 stated that the proposed claim amendments would be entered. As such, it is believed that the proposed claim amendments included in the Supplemental Amendment have been entered.

5. SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention relates generally to a method of forming and/or etching silicon oxide during the fabrication of semiconductor structure, an optical device, or an electromechanical system. (*See Specification*, e.g., page 1, lines 6 to 8).

Independent claim 4 is to a method of forming a silicon oxide layer including positioning a substrate in a deposition chamber and forming a silicon oxide layer by iteratively performing steps multiple times. (*See Specification*, e.g., page 6, lines 4 to 7, 14 to 16.) The iterative steps include oxidizing a silicon precursor gas in the deposition chamber at a first temperature to form a sub-layer of the silicon oxide layer. (*See Specification*, e.g., page 6, lines 19 to 21.) The steps further include providing an oxygen-rich environment in the deposition chamber during the oxidization of the silicon precursor gas. (*See Specification*, e.g., page 16, lines 15 to 16.) The steps further include heating the substrate to a second temperature higher than the first temperature to anneal the sub-layer of the silicon oxide layer. (*See Specification*, e.g., page 6, lines 11 to 13, and page 16, lines 8 to 9.) The steps further include providing an oxygen-rich environment in the deposition chamber during the heating of the substrate. (*See Specification*, e.g., page 16, lines 15 to 16, page 17, lines 3 to 5 and 21 to 22.) The formation of each of the sub-layers formed subsequent to a first one of the sub-layers, the first sub-layer having been formed prior to all of the other of the sublayers, is directly on a respective previously formed one of the sub-layers. (*See Specification*, e.g., page 23, lines 10 to 15.) The second temperature is approximate to the highest processing temperature subsequently applied to the substrate following formation of the silicon oxide layer. (*See Specification*, e.g., page 6, lines 21 to 24, and page 18, lines 7 to 9.)

Independent claim 11 is to a method of forming a silicon oxide layer, including positioning a substrate in a deposition chamber. (*See Specification*, e.g., page 6, lines 4 to 7.) The method further includes oxidizing a silicon precursor gas in the deposition chamber at a first temperature to form a silicon oxide layer. (*See Specification*, e.g., page 6, lines 19 to 21.) The method further includes heating the substrate to a second temperature higher than the first temperature to anneal the silicon oxide layer. (*See Specification*, e.g., page 6, lines 11 to 13, and page 16, lines 8 to 9.) The silicon layer is formed with a compressive stress, such that following the step of heating the substrate, the silicon oxide layer has very low internal stress. (*See Specification*, e.g., page 7, lines 7 to 10, and page 18, lines 12 to 14).

Independent claim 16 is to a method of forming a microelectromechanical systems (MEMS) including forming a MEMS structure on a substrate. Thereafter, the substrate is positioned in a deposition chamber; the silicon precursor gas is oxidized in the deposition chamber at a first temperature to form a silicon oxide layer; and thereafter, the substrate is heated to a second temperature higher than the first temperature to anneal the silicon oxide layer. (*See Specification*, e.g., page 6, lines 11 to 24 and page 7, lines 1 to 2.)

Independent claim 44 is to a method of forming a silicon oxide layer including positioning a substrate in a deposition chamber and forming a silicon oxide layer by iteratively performing steps multiple times. (*See Specification*, e.g., page 6, lines 4 to 7, 14 to 16.) The iterative steps include decomposing a silicon precursor gas in the deposition chamber at a first temperature to form a sub-layer of the silicon oxide layer. (*See Specification*, e.g., page 6, lines 5 to 7.) The steps further include providing an oxygen-rich environment in the deposition chamber during the oxidization of the silicon precursor gas. (*See Specification*, e.g., page 16, lines 15 to 16.) The steps further include heating the substrate to a second temperature higher than the first temperature to anneal the sub-layer of the silicon oxide layer. (*See Specification*, e.g., page 6, lines 11 to 13, and page 16, lines 8 to 9.) The steps further include providing an oxygen-rich environment in the deposition chamber during the heating of the substrate. (*See Specification*, e.g., page 16, lines 15 to 16, page 17, lines 3 to 5 and 21 to 22.) The formation of each of the sub-layers formed subsequent to a first one of the sub-layers, the first sub-layer having been formed prior to all of the other of the sublayers, is directly on a respective previously formed one of the sub-layers. (*See Specification*, e.g., page 23, lines 10 to 15.) The second temperature is approximate to the highest processing temperature subsequently applied to the substrate

following formation of the silicon oxide layer. (*See Specification*, e.g., page 6, lines 21 to 24, and page 18, lines 7 to 9.)

Independent claim 51 is to a method of forming a silicon oxide layer including positioning a substrate in a deposition chamber and forming a silicon oxide layer by iteratively performing steps multiple times. (*See Specification*, e.g., page 6, lines 4 to 7, 14 to 16.) The iterative steps include decomposing a silicon precursor gas in the deposition chamber at a first temperature to form a sub-layer of the silicon oxide layer. (*See Specification*, e.g., page 6, lines 5 to 7.) The steps further include heating the substrate to a second temperature higher than the first temperature to anneal the sub-layer of the silicon oxide layer. (*See Specification*, e.g., page 6, lines 11 to 13, and page 16, lines 8 to 9.) The formation of each of the sub-layers formed subsequent to a first one of the sub-layers, the first sub-layer having been formed prior to all of the other of the sublayers, is directly on a respective previously formed one of the sub-layers. (*See Specification*, e.g., page 23, lines 10 to 15.) The silicon oxide layer is formed with a compressive stress, such that following the step of heating the substrate, the silicon oxide layer has very low internal stress. (*See Specification*, e.g., page 7, lines 7 to 10, and page 18, lines 12 to 14.)

Finally, the appealed claims include no means-plus-function language and no step-plus-function claims, so that 41.37(v) is satisfied as to its specific requirements for such claims, since none are present here.

6. GROUNDS OF REJECTIONS TO BE REVIEWED ON APPEAL

A. Whether claims 4, 11, 44, and 51, which stand rejected under 35 U.S.C. § 103(a), are unpatentable over the combination of the "Yu" and "Ito" references.

B. Whether claims 16 to 18, 22 to 24, 26, 29, and 30, which stand rejected under 35 U.S.C. § 103(a), are unpatentable over the combination of the "Yu" and "Polson" references.

C. Whether claims 19 and 25, which stand rejected under 35 U.S.C. § 103(a), are unpatentable over the combination of the "Yu," "Polson," and "Watanabe" references.

D. Whether claims 20 and 21, which stand rejected under 35 U.S.C. § 103(a), are unpatentable over the combination of the "Yu," "Polson," "Watanabe," and "Torek" references.

E. Whether claims 27, 28, and 56, which stand rejected under 35 U.S.C. § 103(a), are unpatentable over the combination of the "Yu," "Polson," "Watanabe," "Torek," and "Chen" references.

7. ARGUMENTS

A. Rejection of Claims 4, 11, 44, and 51 under 35 U.S.C. § 103(a)

Claims 4, 11, 44, and 51 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of the "Yu" and "Ito" references.

To reject a claim under 35 U.S.C. § 103(a), the Office bears the initial burden of presenting a *prima facie* case of obviousness. *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish *prima facie* obviousness, three criteria must be satisfied.

First, there must be some suggestion or motivation to modify or combine reference teachings. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). As clearly indicated by the Supreme Court, it is "important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the [prior art] elements" in the manner claimed. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727 (2007). In this regard, the Supreme Court further noted that "rejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.*, at 1396.

Second, there must be a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986).

Third, the prior art reference(s) must teach or suggest all of the claim features. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

i. Claim 4

Claim 4 provides that the second temperature to which the substrate is heated to anneal the sub-layers is approximate to the highest processing temperature subsequently applied to the substrate following formation of the silicon oxide layer. In the Final Office Action, the Examiner conclusorily asserts that column 10, lines 4 to 12 and 49 to 55 of the "Yu" reference discloses this feature. Specifically, the Examiner relies on the reference in "Yu" to 920 degrees as disclosing the "highest processing temperature." In fact, the cited section does not refer to the temperature of 920 degrees. Instead, a reference to 920 degrees is made once in the "Yu" reference at column 9, line 10. The reference there is to a temperature employed during the formation of the silicon oxide layer and it is not a discussion of a processing temperature that is reached subsequent to the formation of the silicon oxide layer (which formation is relied upon by the Examiner as assertedly disclosing the formation of the silicon oxide layer of claim 4). Indeed, nowhere does the "Yu" reference disclose or suggest forming a silicon oxide layer which includes heating a substrate to anneal a sub-layer of the silicon oxide layer, where the temperature to which the substrate is heated for the annealing is approximate to a highest processing temperature applied subsequent to the forming of the silicon oxide layer, as provided for in the context of claim 4.

In the first Advisory Action, dated February 26, 2009, the Examiner asserts that "Yu clearly teaches forming a silicon oxide layer at a first temperature (e.g., 920 C)," and further refers to column 10, lines 56 to 66 of the "Yu" reference as assertedly disclosing the second temperature. However, the discussion in which 920 degrees in mentioned is in reference to described example 1, while the cited section pertains to examples 3 and 4. Moreover, the discussion at column 10, lines 56 to 66 regarding examples 3 and 4 do not appear to refer to an oxidizing step, which is the step in claim 4 that refers to the first temperature. Thus, the discussion regarding 920 degrees cannot be relied upon as assertedly disclosing the first temperature of claim 4, where the discussion at column 10, lines 56 to 66 is relied upon as assertedly disclosing the second temperature of claim1.

Regardless, nowhere does the "Yu" reference state that a temperature used for annealing is higher than another temperature used for oxidizing and is the highest processing temperature subsequent to annealing.

The secondary "Ito" reference does not cure the critical deficiencies of the "Yu" reference. While the Advisory Action of February 26, 2009 asserts that column 3, line 64 to column 4, line 4, and column 4, lines 9 to 65 of the "Ito" reference disclose these

features, any review of the cited sections makes plain that they do not at all relate to these features of claim 4. The cited sections make no reference to oxidation. Additionally, while the cited sections state that a heat treatment is performed at 800 degrees, the cited sections do not state that this temperature is higher than that used for an oxidizing step and is approximate to a highest processing temperature applied subsequent to a forming of a silicon oxide layer.

Accordingly, the combination of the "Yu" and "Ito" references does not disclose or suggest all of the features recited in claim 4, so that the combination of the "Yu" and "Ito" references does not render unpatentable claim 4.

Reversal of this obviousness rejection as applied to claim 4 is therefore respectfully requested.

ii. Claim 11

Claim 11 relates to a method of forming a silicon oxide layer and provides for forming a silicon oxide layer with a compressive stress and heating a substrate to anneal the silicon oxide layer. Nothing in the "Yu" reference discloses or suggests forming a silicon oxide layer with a compressive stress, as provided in the context of the claimed subject matter. The secondary "Ito" reference does not cure, and is not asserted to cure, this critical deficiency of the primary reference. The Advisory Action of February 26, 2009 notes that one who performs the steps of a process must necessarily produce all of its advantages. However, the cited references do not disclose performing the required steps for forming a silicon oxide layer with a compressive stress. It is noted that not every formation of a silicon oxide layer results in its formation with a compressive stress.

Thus, the combination of the "Yu" and "Ito" references does not disclose or suggest all of the features recited in claim 11, so that the combination of the "Yu" and "Ito" references does not render unpatentable claim 11.

Reversal of this obviousness rejection as applied to claim 11 is therefore respectfully requested.

iii. Claim 44

Claim 44 provides that the second temperature to which the substrate is heated to anneal the sub-layers is approximate to the highest processing temperature subsequently applied to the substrate following formation of the silicon oxide layer. As explained above as to claim 4, the combination of the "Yu" and "Ito" references does not disclose or suggest this feature.

Therefore, the combination of the "Yu" and "Ito" references does not disclose or suggest all the features of claim 44, so that the combination of the "Yu" and "Ito" references does not render unpatentable claim 44.

Reversal of this obviousness rejection as applied to claim 44 is therefore respectfully requested.

iv. Claim 51

Claim 51 provides for forming a silicon oxide layer with a compressive stress. As explained above as to claim 11, even if the relied upon section of the "Yu" reference may suggest that little additional tensile stress is introduced, it does not identically disclose forming a layer with a compressive stress. Indeed, any review of the "Yu" reference makes plain that it does not identically disclose or suggest this feature. The secondary "Ito" reference does not cure, and is not asserted to cure, this critical deficiency of the primary reference.

Thus, the combination of the "Yu" and "Ito" references does not disclose or suggest all the features of claim 51, so that the combination of the "Yu" and "Ito" references does not render unpatentable claim 51.

Reversal of this obviousness rejection as applied to claim 51 is therefore respectfully requested.

B. Rejection of Claims 16 to 18, 22 to 24, 26, 29, and 30 under 35 U.S.C. § 103(a)

Claims 16 to 18, 22 to 24, 26, 29, and 30, stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of the "Yu" and "Polson" references.

i. Claims 16 to 18, 23, 24, 26, and 29

Claim 16 relates to a method of forming a MEMS and provides for forming a MEMS structure on a substrate, oxidizing a silicon precursor gas to form a silicon oxide layer, and heating the substrate to anneal the silicon oxide layer. With respect to the steps of forming and annealing the silicon oxide layer, the Examiner, in the Final Office Action, refers to the "Yu" reference as assertedly disclosing these features. The Examiner admits that the "Yu" reference is unrelated to a MEMS, but instead refers to the "Polson" reference as assertedly disclosing forming a MEMS structure on a substrate. The Examiner further asserts that it would have been obvious to modify the method of the "Yu" reference to include forming a MEMS structure on the substrate as assertedly taught by the "Polson" reference prior to the steps of forming and annealing the silicon oxide.

However, one skilled in the art would not have formed and annealed silicon oxide as in the "Yu" reference to a substrate that includes a MEMS structure since such oxide layers tend to damage MEMS structures, as explained in the Specification, e.g., at page 3, lines 14 to 20. Accordingly, the modification suggested by the Examiner would have been unpredictable in view of the prior art and necessarily relies on improper hindsight reasoning based on the present disclosure.

In the "Response to Arguments" section of the Final Office Action, the Examiner asserts that "*claim 16 does not require formation of a silicon oxide layer on a MEMS structure or even on the substrate. Therefore applicant's arguments are apparently without merit.*" Appellants do not directly address this argument presented in the "Response to Arguments" section because whether or not claim 16 requires formation of a silicon oxide layer is not at issue. Rather, the issue is whether one skilled in the art would have combined the "Yu" and "Polson" references as suggested in the Final Office Action in order to make a *prima facie* case of obviousness against that which is recited in the claim.

In an attempt to make its case of obviousness, the Examiner suggests a combination of the "Yu" and "Polson" references. In support of the argument that one skilled in the art would have made the suggested combination, the Examiner states that one would

have been motivated to modify the method of the "Yu" reference to include forming a MEMS structure on the substrate as in the "Polson" reference. Appellants' counter-argument negates this argument of the Examiner in the Final Office Action. That is, Appellants' argument shows that the Examiner has not provided any sustainable reasoning as to why one skilled in the art would have combined the references as suggested by the Examiner.

Stated otherwise, Appellants have effectively removed the suggested combination of the "Yu" and "Polson" references, so that the suggested combination of the "Yu" and "Polson" references cannot be used to reject claim 16. Since one skilled in the art would not have made the suggested combination of the teachings of the references relied upon by the Examiner to reject claim 16, therefore, the Examiner has yet to provide any reference or combination of references which discloses or suggests the features of claim 16. Therefore, the Examiner failed to make a *prima facie* case of obviousness with respect to claim 16.

As further regards claim 16, in the "Response to Arguments" section of the Final Office Action, the Examiner asserts that "[i]t was well known in the art at the time of the invention to form silicon oxide deposition layers overtop micromechanical chambers followed by annealing." In support of this contention, the Examiner refers to paragraph [0046] of U.S. Patent Application No. 2004/0065932 (the "Reichenbach" reference). It is respectfully submitted that the cited reference does not support the Examiner's assertions. In fact, the cited section of "Reichenbach" makes no reference to the annealing of the oxide layer, but rather of **polysilicon**. In this regard, it is provided that "a deposition layer **32**, in particular of **polysilicon**, is deposited as a deposition layer over the entire surface (FIG.8). (The "Reichenbach" reference, paragraph [0046], (emphasis added).) The deposition layer 32 (polysilicon) is distinct from the oxide layer (30). The cited section relied upon by the Examiner further provides that the "tempering of the **deposition layer 32** can advantageously be done with the aid of the RTP (Rapid Thermal Processing) or RTA (Rapid Thermal Annealing) reactor." (*Id.*, emphasis added.) Thus, the only annealing discussed by the "Reichenbach" reference relates to deposition layer 32 (**polysilicon**) and not the oxide layer (30).

Accordingly, the combination of the "Yu" and "Polson" references does not disclose or suggest all of the features recited in claim 16, so that the combination of the "Yu" and "Polson" references does not render unpatentable claim 16 or any of its dependent claims, e.g., claims 17, 18, 23, 24, 26, and 29.

Reversal of this obviousness rejection as applied to claims 16 to 18, 23, 24, 26, and 29 is therefore respectfully requested.

ii. Claim 22

Claim 22 depends from claim 16 and is therefore allowable for at least the same reasons as claim 16.

Moreover, claim 22 provides that the second temperature to which the substrate is heated to anneal the silicon oxide layer is approximately the highest processing temperature applied to the substrate following the annealing of the silicon oxide layer. The Examiner, in the Final Office Action, refers to column 10, lines 4 to 12 and 49 to 55 of the "Yu" reference as assertedly disclosing this feature. As more fully explained above as to patentability of claim 4, the cited section of the "Yu" reference does not disclose or suggest this feature, and nowhere does the "Yu" reference disclose or suggest this feature.

For this additional reason, the combination of the "Yu" and "Polson" references does not disclose or suggest all of the features of claim 22, so that claim 22 is allowable for this additional reason.

Reversal of this obviousness rejection as applied to claim 22 is therefore respectfully requested.

iii. Claim 30

Claim 30 depends from claim 16 and is therefore allowable for at least the same reasons as claim 16.

Moreover, claim 30 provides for forming a silicon oxide layer with a compressive stress. The Examiner, in the Final Office Action, refers to the "Yu" reference as assertedly disclosing this feature. However, as more fully explained above as to claim 11, even if the relied upon section of the "Yu" reference may suggest that little additional tensile stress is introduced, it does not disclose forming a layer with a compressive stress. Indeed, any review of the "Yu" reference makes plain that it does not disclose or suggest these features.

For this additional reason, the combination of the "Yu" and "Polson" references does not disclose or suggest all of the features recited in claim 30, so that claim 30 is allowable for this additional reason.

Reversal of this obviousness rejection as applied to claim 30 is therefore respectfully requested.

C. Rejection of Claims 19 and 25 under 35 U.S.C. § 103(a)

Claims 19 and 25 were rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of the "Yu," "Polson," and "Watanabe" references.

Claims 19 and 25 ultimately depend from claim 16 and are therefore allowable over the cited references since the "Watanabe" reference does not correct the critical deficiencies of the combination of the "Yu" and "Polson" references explained as to claim 16.

Reversal of this obviousness rejection of claims 19 and 25 is therefore respectfully requested.

D. Rejection of Claims 20 and 21 under 35 U.S.C. § 103(a)

Claims 20 and 21 were rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of the "Yu," "Polson," "Watanabe," and "Torek" references.

Claims 20 and 21 ultimately depend from claim 19 and are therefore allowable over the cited references since the "Torek" reference does not correct the critical deficiencies of the combination of the "Yu," "Polson," and "Watanabe" references explained above as to claim 19.

Reversal of this obviousness rejection of claims 20 and 21 is therefore respectfully requested.

E. Rejection of Claims 27, 28, and 56 under 35 U.S.C. § 103(a)

Claims 27, 28, and 56 were rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of the "Yu," "Polson," "Watanabe," "Torek," and "Chen" references.

i. Claims 27 and 28

Claims 27 and 28 ultimately depend from claim 16 and are therefore allowable over the cited references since the combination of the "Watanabe," "Torek," and "Chen" references does not correct the critical deficiencies of the combination of the "Yu" and "Polson" references explained above as to claim 16.

Moreover, claim 27 (from which claim 28 depends) further provides that etching the silicon oxide layer includes applying a first etching process to the silicon oxide layer which forms an etch residue, oxidizing the etch residue, and applying a second etching process to the oxidized etch residue. The Examiner, in the Final Office Action, relies on a two stage etching process of "Watanabe" (of which the second stage produces an etch residue (see the "Watanabe" reference, column 4, lines 4 to 16)), as assertedly disclosing the first and

second etching processes of claim 27, but admits that the "Watanabe" reference does not disclose oxidizing an etch residue formed by the first etching process. The Examiner instead conclusorily refers to the "Chen" reference as assertedly disclosing this feature.

Contrary to the Examiner's assertion, the cited section of the "Chen" reference (column 2, lines 43 to 49) states that an oxygen plasma is used for removing a photoresist mask which was previously applied for masking an etching pattern. After the removal of the photoresist mask, residue accumulated during the etching is removed. For the removal, the integrated circuit is dipped into a solvent. Nowhere does the "Chen" reference disclose or suggest oxidizing the etch residue.

In the "Response to Arguments" section of the Final Office Action, the Examiner asserts that column 1, lines 48 to 53 of the "Chen" reference discloses oxidizing the etch residue. However, the cited section does not support this assertion. The "Chen" reference merely states that "the polymeric residues which remain after the plasma-enhanced subtractive etching of poly-silicon layers in reactive halogen-containing gases are removed by a combination of ashing in oxygen gas and removal with an organic solvent." (The "Chen" reference, column 1, lines 48 to 53.) It is respectfully submitted that "**ashing in oxygen gas**" does not disclose nor suggest "**oxidizing** the etch residue" as provided in the context of the claimed subject matter.

Furthermore, even if the "Chen" reference does disclose performing the residue removal by oxidizing the residue (which it does not), the suggested modification of the etching of the "Watanabe" reference to include the asserted features of residue removal of the "Chen" reference would still not disclose the features of claim 27. At most, the "Chen" reference indicates that after etching is completed (and after the etching mask is removed), any remaining residue is removed. Thus, if the features of the "Chen" reference are applied to the method of the "Watanabe" reference, the resulting method would provide for performing the two stage etching process of the "Watanabe" reference, subsequently removing an etching mask, and subsequently removing the etch residue which is produced by the second stage of the "Watanabe" reference.

For all of the foregoing reasons, the combination of the "Yu," "Polson," "Watanabe," "Torek," and "Chen" references does not disclose or suggest all of the features recited in claim 27 from which claim 28 depends, so that the combination of the Yu," "Polson," "Watanabe," "Torek," and "Chen" references does not render unpatentable either of claims 27 and 28.

Reversal of this obviousness rejection of claims 27 and 28 is therefore respectfully requested.

ii. Claim 56

Claim 56 depends from claim 16 and is therefore allowable over the cited references since the combination of the "Watanabe," "Torek," and "Chen" references does not correct the critical deficiencies of the combination of the "Yu" and "Polson" references explained above as to claim 16.

Reversal of this obviousness rejection of claim 56 is therefore respectfully requested.

8. CLAIMS APPENDIX

A "Claims Appendix" is attached hereto and appears on the three (3) pages numbered "Claims Appendix 1" to "Claims Appendix 5."

9. EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131 or 1.132. No other evidence has been entered by the Examiner or relied upon by Appellants in the appeal. An "Evidence Appendix" is nevertheless attached hereto.

10. RELATED PROCEEDINGS APPENDIX

As explained above in Section 2, above, "[t]here are no other prior or pending appeals, interferences or judicial proceedings known by the undersigned, or believed by the undersigned to be known to Appellants or the assignee, Bosch, 'which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.'" As such, there are no "decisions rendered by a court or the Board in any proceeding identified pursuant to [37 C.F.R. § 41.37(c)(1)(ii)]" to be submitted. A "Related Proceedings Appendix" is nevertheless attached hereto.

11. CONCLUSION

In view of the foregoing, it is respectfully requested that the rejections of the finally rejected claims 4, 11, 16 to 30, 44, 51, and 56 be withdrawn, and that these claims be allowed as presented.

Respectfully submitted,

/Aaron Grunberger/

Dated: June 8, 2009

By: Aaron Grunbeger, Reg. No. 59,210
Gerard A. Messina
(Reg. No. 35,952)

KENYON & KENYON LLP
One Broadway
New York, New York 10004
(212) 425-7200

CUSTOMER NO. 26646

CLAIMS APPENDIX

4. A method of forming a silicon oxide layer, comprising:

positioning a substrate in a deposition chamber; and

forming a silicon oxide layer by iteratively performing the following steps multiple times:

oxidizing a silicon precursor gas in the deposition chamber at a first temperature to form a sub-layer of the silicon oxide layer;

providing an oxygen-rich environment in the deposition chamber during the oxidization of the silicon precursor gas;

heating the substrate to a second temperature higher than the first temperature to anneal the sub-layer of the silicon oxide layer; and

providing an oxygen-rich environment in the deposition chamber during the heating of the substrate;

wherein:

the formation of each of the sub-layers formed subsequent to a first one of the sub-layers, the first sub-layer having been formed prior to all of the other of the sub-layers, is directly on a respective previously formed one of the sub-layers; and

the second temperature is approximate to the highest processing temperature subsequently applied to the substrate following formation of the silicon oxide layer.

11. A method of forming a silicon oxide layer, comprising:

positioning a substrate in a deposition chamber;

oxidizing a silicon precursor gas in the deposition chamber at a first temperature to form a silicon oxide layer; and

heating the substrate to a second temperature higher than the first temperature to anneal the silicon oxide layer;

wherein the silicon oxide layer is formed with a compressive stress, such that following the step of heating the substrate, the silicon oxide layer has very low internal stress.

16. A method of forming a microelectromechanical systems (MEMS), comprising:

forming a MEMS structure on a substrate; and thereafter,

positioning the substrate in a deposition chamber;

oxidizing a silicon precursor gas in the deposition chamber at a first temperature to form a silicon oxide layer; and thereafter,

heating the substrate to a second temperature higher than the first temperature to anneal the silicon oxide layer.

17. The method of claim 16, further comprising:

providing an oxygen-rich environment in the deposition chamber during the oxidization of the silicon precursor gas.

18. The method of claim 17, further comprising:

providing an oxygen-rich environment in the deposition chamber during the heating of the substrate.

19. The method of claim 18, further comprising:

etching the silicon oxide layer without producing an etch residue.

20. The method of claim 19, wherein etching the silicon oxide layer is performed using one selected from a group consisting of a vapor etch, a wet etch, and a plasma etch.

21. The method of claim 20, wherein etching the silicon oxide layer is performed using an HF-vapor etch.

22. The method of claim 16, wherein the second temperature is approximate to the highest processing temperature applied to the substrate following the annealing of the silicon oxide layer.

23. The method of claim 16, wherein the silicon precursor gas is provided at low pressure.

24. The method of claim 17, wherein the oxygen-rich environment further comprises at least one gas selected from a group of gases consisting of nitrogen, helium, argon, ozone and steam.

25. The method of claim 19, wherein heating the substrate occurs in an environment comprising at least one gas selected from a group of gases consisting of oxygen, nitrogen, helium, argon, ozone and steam.

26. The method of claim 16, wherein the second temperature ranges from 700 to 1200° C.

27. The method of claim 21, wherein etching the silicon oxide layer further comprises:

applying a first etching process to the silicon oxide layer which forms an etch residue;

oxidizing the etch residue; and

applying a second etching process to the oxidized etch residue.

28. The method of claim 27, wherein at least one of the first and second etching processes comprises a HF-vapor etch.

29. The method of claim 16, wherein the silicon precursor gas comprises at least one gas selected from a group of gases consisting of: tetraethoxysilane (TEOS), silane (SiH_4), dichlorosilane (DCS), diethlysilane (DES), and/or tetramethylcyclotetrasiloxane (TOMCATS).

30. The method of claim 16, wherein the silicon oxide layer is formed with a compressive stress, such that following the step of heating the substrate, the silicon oxide layer has very low internal stress.

44. A method of forming a silicon oxide layer, comprising:

positioning a substrate in a deposition chamber; and

forming a silicon oxide layer by iteratively performing the following steps multiple times:

decomposing a silicon precursor gas in the deposition chamber at a first temperature to form a sub-layer of the silicon oxide layer;

providing an oxygen-rich environment in the deposition chamber during the decomposition of the silicon precursor gas;

heating the substrate to a second temperature higher than the first temperature to anneal the sub-layer of the silicon oxide layer; and

providing an oxygen-rich environment in the deposition chamber during the heating of the substrate;

wherein:

the formation of each of the sub-layers formed subsequent to a first one of the sub-layers, the first sub-layer having been formed prior to all of the other of the sub-layers, is directly on a respective previously formed one of the sub-layers; and

the second temperature is approximate to the highest processing temperature subsequently applied to the substrate following formation of the silicon oxide layer.

51. A method of forming a silicon oxide layer, comprising:

positioning a substrate in a deposition chamber; and

forming a silicon oxide layer by iteratively performing the following steps multiple times:

decomposing a silicon precursor gas in the deposition chamber at a first temperature to form a sub-layer of the silicon oxide layer; and

heating the substrate to a second temperature higher than the first temperature to anneal the sub-layer of the silicon oxide layer;

wherein:

the formation of each of the sub-layers formed subsequent to a first one of the sub-layers, the first sub-layer having been formed prior to all of the other of the sub-layers, is directly on a respective previously formed one of the sub-layers; and

the silicon oxide layer is formed with a compressive stress, such that following the step of heating the substrate, the silicon oxide layer has very low internal stress.

56. The method of claim 16, further comprising:

etching the silicon oxide layer, wherein the etching comprises:

applying a first etching process to the silicon oxide layer which forms an etch residue;

oxidizing the etch residue; and

applying a second etching process to the oxidized etch residue.

EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§1.130, 1.131, or 1.132. No other evidence has been entered by the Examiner or relied upon by Appellants in the appeal.

RELATED PROCEEDINGS APPENDIX

As indicated above in Section 2 of this Appeal Brief, "[t]here are no other prior or pending appeals, interferences or judicial proceedings known by the undersigned, or believed by the undersigned to be known to Appellants or the assignee, Bosch, 'which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.'" As such, there are no "decisions rendered by a court or the Board in any proceeding identified pursuant to [37 C.F.R. § 41.37(c)(1)(ii)]" to be submitted.